In the Specification:

Please amend the paragraph beginning on page 1, line 17, as follows:

Generally, a trench is formed by etching an insulating layer, and ~~a~~ an interconnection line is formed in the trench by a self-align dual damascene process.

Please amend the paragraph beginning on page 1, line 20, as follows:

In the self-align dual damascene process, a via connecting the lower and upper interconnection lines is aligned at a bottom of the trench. That is, in the self-align dual damascene process, an insulating layer is selectively etched with ~~the~~ a photolithography process to form a trench exposing a via at the bottom thereof, and a conductive layer is formed with W, Al or Cu to fill the trench. After that, the portion of conductive layer outside of the trench, ~~namely a portion of the conductive layer,~~ which is not necessarily needed, is removed by an etching or a chemical mechanical polishing (CMP) to form ~~a~~ an interconnection line in the trench.

Please amend the paragraph beginning on page 3, line 14, as follows:

Referring to Fig. 1C, a trench 21 is formed by etching the fourth interlayer insulating layer 18 using the trench mask 20. When the trench 21 is formed, the etching is stopped ~~at~~ by the etching stop layer 17.

Please amend again the paragraph beginning on page 3, line 26, as follows:

As shown in Fig. 2A, after forming the trench by etching the fourth interlayer insulating layer 18, the etching stop layer 17 ~~is left~~ remains except at the via hole region. The etching stop layer 17 is usually formed with the nitride layer having a high capacitance value, which in this case, results in a problem of capacitance increase ~~occurs~~ due to the remaining etching stop layer 17.

Please amend the paragraph beginning on page 4, line 10, as follows:

A method for forming multi-level interconnection lines using a dual damascene process is disclosed. With the dual damascene process, it is easy to control distortion of a profile on a corner of a trench, and to prevent the capacitance value from increasing due to a remaining etching stop layer.

Please amend the paragraph beginning on page 5, line 5, as follows:

Other aspects of the disclosed methods will become apparent from the following description with reference to the accompanying drawings, ~~aherein~~ wherein:

Please amend the paragraph beginning on page 5, line 27, as follows:

Referring to Fig. 3A, in a method of manufacturing multi-level metal interconnection lines, interlayer insulating layers 32 and 33 and an etching stop layer 34 are formed on a semiconductor substrate 31. After that, the etching stop layer 34 and the interlayer insulating layer 33 are selectively etched to ~~exposure~~ expose a ~~part~~ via or trench where a metal interconnection line is to be formed.

Please amend again the paragraph beginning on page 8, line 19, as follows:

The metal interconnection lines 35 and 43 and the via 43a may be formed with any one selected from the group consisting of Al, Cu, Au, Ag and Cr. The metal layers are deposited at a thickness ranging from about 2000 Å to about 30000 Å by using any one selected the group consisting of a chemical vapor deposition (CVD), an ~~and~~ electroless deposition and a physical vapor deposition (PVD).

Please amend again the paragraph beginning on page 9, line 5, as follows:

Since the minimum etching stop layer for forming the trench is used by patterning the etching stop layer ~~to remain in~~ so that it remains only around the inlet of the via hole, an increase of capacitance due to the etching stop layer having high capacitance can be prevented. Also, since the interlayer insulating layer having a void is etched to form the trench, a margin of a trench etching process may be maximized.